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(54) **Surface mounting semiconductor device and method.**

(57) A surface mounting device (10) incorporating a high power RF semiconductor transistor comprises a common lead plane (12), an input lead plane (14), a collector lead plane (16), a transistor die (20) electrically and thermally connected to the collector lead plane (16), bonding wires (26,26') for connecting emitters (24) and bases (22) of the transistor (20) to the common (12) and input (14) lead planes respectively, and a molded plastic body member (28) for sealing the device components (70) while leaving the lower coplanar surfaces of the lead planes exposed on the bottom face of the device (11). There are no flying leads.

By eliminating an expensive metallized ceramic insulator from inside the device package (10) and instead providing electrical isolation as a part of an external circuit board (30), the cost for fabricating the device and installing them on the printed circuit board (30) are significantly reduced. The device is particularly rugged and can be easily mounted on the PC board (30) by automated equipment.

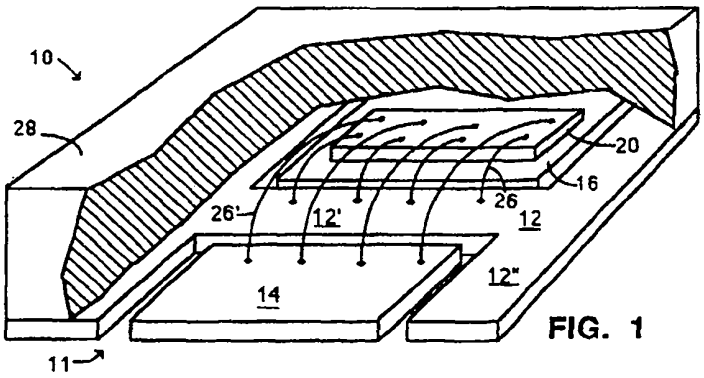

FIG. 1

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SURFACE MOUNTING SEMICONDUCTOR DEVICE

Field of the Invention

The present invention relates, in general, to a surface mounting packaged semiconductor device and, more particularly, to a surface mounting device without an internal insulator under the active element, and a fabrication method therefor.

Background of the Invention

With the increasing use of high power transistors (1 to 80 Watts) in electrical circuits which operate at high frequencies, such as radio frequencies (RF), e.g. 25 MHz to 1GHz, it has become necessary to design transistor packages which permit the transistors to operate properly in such circuits. The packages for such high power transistors must be capable of dissipating the relatively high quantities of heat generated by the transistor to maintain the transistor at a suitable operating temperature, i.e., a temperature which will not adversely affect the operating characteristics of the transistor. Another important characteristic for such packages is that they provide for good electrical grounding of the transistor with a minimum of parasitic inductance.

In order to satisfy these requirements and provide collector isolation, prior art high frequency semiconductor device packages for many high frequency transist,ors utilize internal metallized ceramic insulators. The metallization provides electrical connection to the transistor while the ceramic provide electrical isolation but thermal conduction between, typically, the transistor collector and the underlying heat sink on which the device is ultimately mounted.

For example, U.S. Pat. No. 3,969,752 discloses a semiconductor device package having a metal layer for supporting the bottom of an NPN transistor die and connecting to the transistor, collector, and having a ceramic insulator underlying the collector metal layer and overlying the lowest metal layer functioning as a ground terminal and as a heat sink. The bottom of the transistor die is the collector. This is because a top collector transistor configuration causes large parasitics. However, the collector must be separated from the common or ground terminal which is usually connected to the emitter. Therefore, electrical isolation of the bottom of the transistor from the ground is needed. Another U.S. Pat. No. 3,728,589 describes a semiconductor assembly having a mounting block of an electrical insulating but thermally conducting material, such as beryllium oxide or alumina, mounted in a cavity in a ground plane member.

Although the heat dissipation and the electrical parasitic characteristics of RF transistor device packages have been improved in the prior art, they require additional materials and processes for introducing metallized ceramics, which are time and cost consuming. Insulating BeO and Al_2O_3 ceramics 508 to 1524 mm thick, such as are commonly used in the prior art, are expensive. Further, the ceramic must be metallized, with e.g. gold, and then usually brazed or soldered to other package components. As a result, the final package cost including the cost of the ceramic material, the metallization, brazing or soldering, and the heat sink becomes quite high.

In addition, some prior art semiconductor device packages are prone to have flux and solder enter the cavity of the device, for example, during soldering operations used to attach the packages to the circuit. Further, most prior art RF packages are not well suited for surface mounting and are not designed to be easily handled by pick and place equipment. Also, positioning of capacitors close to most prior art packages is often difficult because of the protruding flying leads found on these packages.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an improved surface mounting semiconductor device and method, therefore including for example a high power transistor adapted for high frequency operation, wherein the cost and time required for fabricating the device are reduced.

More particularly, it is an object of the present invention to provide such a surface mounting semiconductor device and fabricating method thereof, without using an internal insulator under the active element.

Yet another object of the present invention is to provide an improved electronic assembly including such device and a mating printed circuit board having an electrically insulated heat sink, wherein the total cost is reduced.

In carrying out the above and other objects of the invention, there is provided in an exemplary embodiment employing a transistor, a surface mounting package for a high power semiconductor

device comprising a common lead plane, an input lead plane, a collector lead plane, a transistor die mounted on the collector lead plane, bonding wires for connecting emitter(s) and base(s) of the transistor to the common and input lead planes respectively, and an enclosure for sealing the package components. By removing the expensive metallized ceramic insulator from within the device package and instead forming the collector isolation insulator as a part of a printed circuit board or as an insert in the circuit board, the cost of fabricating the device package is significantly reduced. Further, the device of the present invention can be conveniently handled by pick and place equipment because it need not have flying leads typical of prior art dual-in-line or gull-wing or SOT type packages.

In accordance with another feature of the present invention, there is also provided an electronic assembly comprising such device and a printed circuit board. For the situation where the device comprises a transistor, the printed circuit board has a board member of insulating material, a common contact, an input contact and an output contact on the board member, and a thermally conductive region extending through the board member whose upper surface is desirably coplanar with the upper surface of the contacts. The device package is mounted on the printed circuit board so that the common, input and a first portion of the collector lead planes are in contact with the common, input and output contacts respectively, and another portion of the collector lead plane is in contact with the heat sink region. Because the heat sink member need incorporate only a very thin electrical insulator, and because it can be placed in or on the printed circuit board without need of metallizing or, alternatively, provided as a separate part, the required processes and the total cost for making such electric circuit (including the device, the printed circuit board and the heat sink member) is reduced.

These and other objects and advantages will be apparent to one of skill in the art from the detailed description below taken together with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a partially cut away and perspective view illustrating a surface mounting electronic device according to one embodiment of the present invention;

FIG. 2 is a simplified plan view of a leadframe with lead planes, a transistor die and wire bonds, such as is incorporated in FIG.1;

FIG. 3A is a cross-sectional view of the device shown in FIG.1 and a printed circuit board containing a heat sink insulator, illustrating the contacting relationship between the device and the printed circuit board;

FIGS. 3B-D are simplified cross-sectional drawings of alternative heat sink insulators that can be utilized in FIG. 3A;

FIG. 4 is a perspective view of a printed circuit board and device similar to that shown in FIG. 3A but according to a further embodiment of the present invention;

FIG. 5 is a cross-sectional view of an additional embodiment of a printed circuit board similar to that shown in FIG. 3A;

FIGS. 6A-8A are simplified plan views of various lead planes with transistor die thereon, according to still further embodiments of the present invention; and

FIGS. 6B-8B are simplified central cross-sections of FIGS. 6A-8A, respectively.

DETAILED DESCRIPTION OF THE INVENTION

A semiconductor device suitable for mounting to a mating printed circuit board, according to the present invention, will now be described in detail with reference to a preferred embodiment thereof, illustrated in FIGS. 1, 2 and 3. Alternative configurations are illustrated in FIGS. 4-6. The present invention is useful for discrete transistors and ICs and is especially well suited to RF power devices and circuits.

For convenience of explanation and not intended to be limiting, the package and circuit arrangement is described herein in terms of a bipolar transistor having emitter, base and collector terminals. However, those of skill in the art will understand that the present invention also applies to other electronic elements, such as for example, field effect transistors, thyristors, diodes, phototransistors, and other elements familiar to those of skill in the art. As used herein, the words "transistor" or "transistors" are intended to include such other elements and the words "emitter", "base", and/or "collector" are intended to include analogous terminals of such other elements.

Referring now to FIGS. 1-3A, surface mountable electronic device 10 includes substantially flat common lead plane 12 exposed on lower face 11 of device 10 and having upper and lower surfaces. Common lead plane 12 comprises in the illustrated embodiment, two parallel side portions 12" joined by bridge portion 12', and is made of an electrically conductive material, such as copper.

Device 10 also includes input lead plane 14 whose lower surface is also exposed on lower surface 11 of device 10. Input lead plane 14 is,

preferably, a flat rectangular electrode having upper and lower surfaces, and is made of an electrically conductive material, such as copper. However, common and input lead planes 12 and 14 may be made of other materials covered with an electrically conducting material.

Device 10 further includes collector lead plane 16 whose lower surface is also exposed on lower surface 11 of device 10 in the same manner as lead planes 12, 14. Collector lead plane 16 is, preferably, a flat rectangular electrode having upper and lower surfaces and, desirably, has an area which is large compared to transistor die 20. Collector lead plane 16 is made of an electrically and thermally conductive material, such as copper. However, collector lead plane 16 may be made of a good thermally conductive material which is coated with an electrically conductive layer.

The lower surfaces of lead planes 12, 14 and 16 are substantially coplanar and are exposed on or slightly protrude from surface 11 of device 10. For manufacturing convenience, leads 12, 14 and 16 may be part of a planar "ladder" lead-frame with detachable side-rails 13 and support strips visible in FIG. 2, which are sheared off after encapsulation. While leads 12 14, 16 are shown as having a shape that is rectangular or a combination of joined rectangles and as having the same thickness, they may have any convenient lateral shape and variable thickness. It is important however that their lower surfaces be substantially flat and coplanar.

Transistor die 20 is generally a flat body of semiconductor material, such as for example a silicon chip having several bipolar transistor cells or other device regions formed therein. The number of cells and type of transistor or other element will vary with particular applications. For example, RF transistors having from 1 to 40 NPN amplifying cells are commonly used. Such devices are constructed by means well known in the art. Multiple parallel wire bonds are typically used to connect the device regions of the cells to the package leads.

Transistor die 20 is mechanically secured to the upper surface of collector lead plane 16 by any convenient method, such as for example, bonding with Au-Ge or Au-Si eutectic or other suitable electrically and thermally conductive attachment material. Thus, the lower surface of transistor die 20 is electrically and thermally coupled to the upper surface of collector lead plane 16. In the embodiment shown in FIGS. 1-2, four transistor cells are illustrated, i.e., four emitter electrode regions 24 and four base electrode regions 22 are provided on the upper surface of transistor die 20. A collector electrode region (not shown) is provided on the lower surface of transistor die 20, and is electrically and thermally coupled to the upper surface of collector lead plane 16. Transistor die 20 is generally smaller in area than the upper surface of collector lead plane 16.

Although transistor die 20 is shown as being positioned adjacent one edge of collector lead plane 16, it may be placed anywhere on the upper surface of collector lead plane 16. Further, while die 20 is referred to for convenience as a transistor, it may be any electronic element having at least two terminals, wherein the surface bonded to lead 16 is the principal heat dissipating surface.

Where the transistor contained within package 10 is to be used in the common emitter configuration, which is typical in RF amplifiers, emitter contact regions 24 of transistor die 20 are electrically connected to the upper surface of bridge portion 12′ of common lead plane 12 by a plurality of bonding wires 26. Wires 26 are of an electrically conductive metal, such as gold or aluminum. Wires 26 are bonded preferably by either ultrasonic or compression bonding techniques.

Base contact regions 22 of transistor die 20 are electrically connected to the upper surface of input lead plane 14 by a plurality of bonding wires 26′ similar to wires 26. While gold and aluminum wire are particularly convenient for connections 26, 26′, other interconnection means well known in the art may also be used. As used herein the words "bonding wires" are intended to refer generally to any means of interconnecting the wire bonding pads or attachment points on the semiconductor die to the appropriate regions on the lead planes.

Although the common emitter configuration is illustrated in FIGS. 1, 2 and 3, it should be understood that the present invention is not limited to this configuration and is also useful in a common base configuration. In such common base configuration, base contact regions 22 are connected to bridge portion 12′ of common lead plane 12, and emitter regions 24 are connected to input lead planes 14. In either configuration, collector lead plane 16 would provide the electrical terminal of the collector of the transistor and the principal thermal dissipation heat path. The lead arrangement of device 10 is easily modified to accept a top-side collector die in which case bonding wires or equivalent would be used for coupling the top collector contact to lead plane 16. Further, while it is convenient to connect bonding wires 26 to bridge portion 12′ of common lead plane 12, this is not essential and wires 26 may extend to side portions 12″ of lead plane 12.

Where a two-terminal element (e.g. a diode) is desirable to be used as die 20, then it would be mounted on the lead plane intended to serve as the principal thermal dissipation leas (e.g. lead plane 16), and wire bonded, for example, to an

input lead plane (e.g. 12 and/or 14). Either or both of lead plane 12, 14 may be as the input lead plane or they may be combined.

Device 10 further comprises body or encapsulation 28 which provides primary structural support for device 10 and its interior parts, and protects the interior parts from the ambient atmosphere and from mechanical damage. Body 28 is preferably made of a moldable compound, for example, a thermo-setting plastic, formed by conventional molding techniques, such as injection molding. Body 28 desirably encapsulates bonding wires 26,26′ die 20 and the upper surfaces of lead planes 12, 14 and 16. However, the lower surfaces of lead planes 12, 14 and 16 are exposed to allow electrical connection to the device. Portions of the lateral edges of leads 12, 14, 16 may or may not be exposed. Either arrangement works. Particular features of device 10, according to the present invention, are that it is capable of being tested prior to mounting onto a printing board circuit and that it is well adapted for handing by automatic machinery because it is free from the flying leads that protrude a significant distance from the package and which

FIG. 3A illustrates a cross-sectional view of device 10 and its mating printed circuit board 30. Printed circuit board 30 is preferably composed of an epoxy glass insulating base material with electrical connection patterns formed on its upper and/or lower surface. Such circuit boards are well known in the art.

The insulating base material may be considered to be made up of three portions, that is, common portion 32, input portion 33 and output portion 36. On these portions there are respectively provided common contact 34, input contact 44 and output contact 46, so positioned as to mate with common lead plane 12, input lead plane 14 and a portion of collector lead plane 16, respectively, when package 10 is mounted on board 30. Contacts 34, 44 and 46 are typically made of a thin electrically conductive material, such as copper foil or gold plated copper foil and are separated from each other like islands. The contact configuration may be varied according to the connections. FIG. 4 illustrates another contact configuration of printed circuit board 30 and FIGS. 6A-8A illustrate alternative lead plane and transistor configurations. Printed circuit board 30 is usually fixed on another heat sink structure, such as chassis 42, as shown in FIG. 3A.

In a first embodiment, recess portion 38 is provided between common portion 32 and output portion 36, extending through the insulating base material. Electrically insulating and thermally conducting heat sink plate 40 having a flat upper surface is inserted into recess portion 38 so as to mate with lead plane 16, preferably just under transistor die 20, when device 10 is mounted on board 30.

Heat sink plate 40 contains an electrically insulating but thermally conductive material, preferably a highly thermally conductive ceramic such as Al_2O_3 or BeO. This provides electrical insulation while allowing thermal conduction to extract the heat dissipated during operation of transistor die 20. Although heat sink plate 40 preferably contains alumina or beryllium oxide, other suitable thermally conductive but electrically insulating materials could be used.

Heat sink plate 40 may be homogeneous, as shown for example in FIG. 3A or be laminated, as shown for example in FIGS. 3B-D. In FIGS 3B-D, heat sink plate 40 comprises highly thermally conductive metal regions 401 and electrically insulating but thermally conductive region 402. Other combinations may also be used. Because heat sink plate 40 may be formed using only very thin ceramic, e.g., 25.4-127.0 mm as opposed to 508-1016 mm for the typical in-package isolators, the cost for such expensive ceramic materials can be reduced. Further, assembly of heat sink plate 40 on board 30 is much less critical than placing an equivalent electrical isolation element under the semiconductor die within the prior art packages.

The upper surface of contacts 34, 44 and 46 and heat sink plate 40 may be coated with a metal adapted to permit the lower surfaces of lead planes 12, 14 and 16 to be well bonded to contacts 32, 34 and 36 and heat sink plate 40 with a suitable solder or other electrical connection means. Contacts 34, 44 and 46 are desirably a of a highly electrically conductive metal, such copper, gold or gold plated copper so as to provide a low inductance. This is important where RF operation is desired.

Instead of forming recess portion 38 for receiving heat sink plate 40, metal region 40′ may be provided on the upper surface of board 30 between common contact 34 and output contact 46 as shown in FIG. 5. In this situation, the dielectric material of board 30 serves as the thermal conductor to remove heat from lead plane 16 under die 20. This method is usually thermally less effective because most common board materials (e.g., glass loaded plastics) have lower thermal conductivity than ceramics such as BeO or alumina. However, the cost is substantially lower because the expensive ceramic plate is eliminated and heat transfer is still better than would be obtained without the PC board under lead 16.

Device 10 is desirably mounted on printed circuit board 30 so that heat sink plate 40, 40′ is located immediately beneath transistor die 20. Heat sink plate 40, 40′ should have as large an area as is practical without interfering with leads 12 and 16

since this decreases the thermal impedance.

Referring to FIG. 3A, when device 10 and board 30 are combined, the lower surfaces of lead planes 12, 14, 16 are substantially coplanar with the upper surface of the leads and heat-sink region on printed circuit board 30. That is, common, input and collector lead planes 12, 14 and 16 are in electrical contact with contacts 34, 44 and 46 respectively, and lead plane 16 is also in thermal contact with heat sink plate 40. It is desirable that lower surface 11 of package encapsulation 28 be recessed slightly (e.g., 12.70127.0 mm) from the lower surface of lead planes 12, 14, 16 so as to insure that no part of encapsulation 28 interferes with contact between lead planes 12, 14, 16 and board contacts 44, 34, 40 and 46.

Because the principal heat dissipating electrode of die 20 is separated from heat sink plate 40 in printed circuit board 30 only by metallic lead 40 (and any joining solder materials) and heat sink plate 40 is well coupled thermally to heat sink 42, a very low impedance heat dissipation path is obtained. Also, since lead 16 and heat sink plate 40 can have a larger area than die 20, substantial heat spreading can occur, further reducing the thermal impedance.

Advantages of the present invention are that (i) collector lead plane 16 serves as the support for die 20, as the electrical connector to the lower face of die 20 and as a heat path to provide excellent heat dissipation from die 20 to heat sink 42, (ii) very short wires 26, 26′ may be used for connecting device regions on die 20 (or other components) to lead planes 12, 14, and (iii) device 10 mounts directly onto contacts 34, 44, 46 and heat sink plate 40. As a consequence, the parasitic resistance and inductance and the thermal impedance are minimized. These features are extremely useful, especially in RF applications. Accordingly this invention provides an electronic device wherein a transistor or IC or other component or combination thereof can operate at radio frequencies at high powers with the achievement of high gains at high efficiencies and good stability.

FIGS. 6A-8A show plan views in simplified form analogous to FIG. 2, but of alternative lead arrangements. FIGS. 6B-8B show simplified central cross-sections of the lead plane arrangements of FIGS. 6A-8A viewed from the right side thereof and analogous to the cross-section of device 10 shown in the upper portion of FIG. 3A but with encapsulation 28 shown by the dashed lines. In FIGS. 6A-8A, the letters G, E, C and B designate which of the lead planes is coupled to the ground (common), emitter, collector and base terminals of the die, respectively. As those of skill in the art will appreciate based on the description herein, this is merely for ease of explanation and not intended to be limiting.

FIGS. 6A-6B shows an arrangement similar to that in FIGS. 2-3A but with the addition of MOSCAP 52, i.e. an MOS device serving as a capacitor. Bonding wires 54, 56, 58 interconnect die 20, MOSCAP 52 and lead planes 12, 14. MOSCAP 52 typically has one electrode directly connected to lead plane 12, as illustrated.

FIGS. 7A-B shows another arrangement in which common or ground lead plane 12 has bridge portion 62 extending over collector lead 16 so as to permit a double bonded, grounded emitter configuration.

FIGS. 8A-8B show a further arrangement in which a yoke-shaped collector and emitter are provided with double bonded emitters and additional components 70, e.g., resistors, inductors and/or capacitors. While components 70 are indicated as being all alike, those of skill in the art will appreciate that there may be different components or values in different locations. By varying the connections between lead planes 12, 14, 16 and die 20, MOSCAP 52 and components 70, many different electrical circuits can be provided within device 10.

Where a two-terminal element (e.g. a diode) is desirable to be used as die 20, then it would be mounted on the lead plane intended to serve as the principal thermal dissipation lead (e.g. lead plane 16), and wire bonded, for example, to an input lead plane (e.g. 12 and/or 14). Either or both of lead plane 12, 14 may be as the input lead plane or they may be combined.

Electronic device 10 of the present invention is conveniently formed by a method comprising, providing first lead planes 12 of an electrically conductive material (e.g., copper) having opposed first and second surfaces, providing second lead plane 16 of an electrically conductive material (e.g., copper) having opposed first and second surfaces, providing semiconductor die 20 including a first surface having at least one device region therein and a second surface opposite the first surface, attaching the second surface of the semiconductor die to the first surface of second lead plane 16 without an intervening insulator, connecting the at least one device region to the first surface of first lead plane 12 (e.g., by wire 26), and encapsulating device 10 so that at least portions of the second surfaces of lead planes 12, 16 are exposed on a first face of the encapsulation. The second faces of lead planes 12, 16 are exposed. Their edges (e.g., see FIG. 1) may also be exposed.

It is desirable that the foregoing steps provide exposed second surfaces of lead planes 12, 16 that are substantially flat and coplanar. It is further desirable that the encapsulating step provide an encapsulation body that is recessed slightly from the exposed second surfaces of the lead planes. It

is further desirable that lead planes 12, 14 form part of a planar "ladder" leadframe having supporting side-rails 13 which are sheared off after encapsulation.

An electronic assembly having a surface mounting device and a printed circuit board for receiving the device thereon, is formed by the method comprising:

(A) providing surface mounting device 10 comprising, first lead plane 12 of an electrically conductive material having opposed first and second surfaces, second lead plane 16 of an electrically conductive material having opposed first and second surfaces, semiconductor die 20 including a first surface having at least one device region therein and a second surface opposite the first surface, wherein the second surface of semiconductor die 20 is coupled to the first surface of the second lead plane without an intervening insulator, connecting means 26 for electrically coupling the at least one device region to the first surface of first lead plane 12, and encapsulation body 28 for providing structural support for device 10, wherein body 28 covers connecting means 26, semiconductor die 20, and the first surfaces of lead planes 12, 16, and wherein at least parts of the second surfaces of lead planes 12, 16 are exposed on a first face of body 28 (e.g., surface 11 of device 10); and

(B) providing printed circuit board 30 comprising, a board member made of an electrically insulating material and having a major surface, first contact 34 of an electrically conductive material and positioned on the surface of the board member so as to mate with at least part of the exposed second surface of the first lead plane 12, second contact 46 of an electrically conductive material and positioned on the surface of the board member so as to mate with at least a first part of the exposed second surface of the second lead plane 16, thermally conductive region 40 extending through the board member and positioned to mate with at least a second part of the exposed second surface of the second lead plane 16 different than the first part thereof, and

(C) mounting device 10 on printed circuit board 30 with the second surfaces of first and second lead planes 12, 16 at least partially contacting first and the second contacts 34, 46, respectively, and the second surface of second lead plane 16 at least partially contacting thermally conductive region 40.

It is desirable that thermally conductive region 40 be of a material different than circuit board 30, e.g., of a more thermally conductive material than the insulating base material of circuit board 30, and that it extend through circuit board 30.

Advantages

According to the present invention, the cost of the surface mounting packages can be remarkably reduced, because the costly metallized ceramic insulator commonly placed between the semiconductor die and the leadframe in prior art packages is no longer required. Even if the same costly ceramic insulator is used as the heat sink plate in the PC board, there is a substantial material saving associated with those encapsulated semiconductor devices that fail final test and are discarded since there is no need to discard the costly ceramic along with the defective device.

Further, the heat sink material which is now incorporated in the printed circuit board, can be made thinner (25.4-127.0 mm versus 508-1016 mm) and does not require intricate processes such as metallization or brazing. Therefore, the total cost for assembling the electrical circuit including the package and the printed circuit board can be also reduced.

The manufacture of the invented device can be easily automated because a convenient flat "ladder" strip type leadframe may be used. Low cost plastic encapsulation of ladder leadframes and components thereon is well known in the art.

Once manufacturing is completed, the lack of flying leads makes the finished device particularly easy to handle. Bent and damaged leads are avoided since only flat faces of the leads are exposed on package surface 11 and they are held firmly in place by body 28. There are no protruding gull-wing or "J" leads or other types of flying leads to be bent. These features combine to make the invented device particularly convenient for surface mounting on PC boards using automated pick and place equipment.

A further feature of the present invention is that the various lead planes which support the internal die and wires and provide for external connection to the package are held together by encapsulation 28. Thus, a separate supporting substrate is not needed as a part of the device package.

Further, the arrangement provides great flexibility of device and package design so that not only can surface mount devices be constructed according the principles of the present invention, but more conventional parts can also be realized. For example, where the invented device is desired to provide a drop-in replacement for a prior art flying lead device, it may be readily converted to a flying lead device by attaching flying leads to exposed lead planes 12, 14, 16.

While the present invention has been shown and described with reference to particular embodiments thereof, various additional modifications and changes will be apparent to those skilled in the art, based on the description herein. For example, while the invented device has been described as employing bipolar transistors, those of skill in the art will understand that any component having two or more terminals may be employed as die 20 and that the present invention is not limited to three terminal devices. Accordingly, it is intended to include within the scope of the claims that follow these and such other variations as will occur to those of skill in the art based on the description herein.

Claims

1. A method for providing an electronic device (10), characterized by:
providing a first lead plane (12) of an electrically conductive material having opposed first and second surfaces;
providing a second lead (16) plane of an electrically conductive material having opposed first and second surfaces;
providing a semiconductor die (20) including a first surface having at least one device region therein and a second surface opposite the first surface;
attaching the second surface of the semiconductor die (20) to said second lead plane (16) without an intervening insulator;
connecting said at least one device region to said first lead plane (12); and
encapsulating the device (10) so that at least portions of said second surfaces of said lead planes (12, 16) are exposed on a first face of said body and not elsewhere.

2. A method of forming an electronic assembly comprising a surface mounting device (10) and a printed circuit board (30) for receiving said device (10) thereon, characterized by:
(A) providing said surface mounting device (10) comprising:
a first lead plane (12) of an electrically conductive material having opposed first and second surfaces;
a second lead plane (16) of an electrically conductive material having opposed first and second surfaces;
a semiconductor die (20) including a first surface having at least one device region therein and a second surface opposite the first surface with the second surface coupled to said second lead plane (16) without an intervening insulator;
connecting means (26) for electrically connecting said at least one device region to said first lead plane (12);
a body (28) for providing structural support for the device (10), said body (28) covering said connecting means (26,26′) and said first surfaces of said lead planes (12,14,16) and said semiconductor die (20), wherein at least portions of said second surfaces of said lead planes (12,14,16) are exposed on a first face of said body (28); and
(B) providing said printed circuit board (30) comprising:
a board member (32) made of an electrically insulating material and having a surface;
a first contact (34) of an electrically conductive material, positioned on the surface of said board member (32) so as to mate with at least part of the exposed second surface of said first lead plane (12);
a second contact (46) of an electrically conductive material, positioned on the surface of said board member (36) so as to mate with at least a first part of the exposed second surface of said second lead plane (16);
a thermally conductive region (402) extending through the board member (40) and positioned to mate with at least a second part of the exposed second surface of the second lead plane (16), different than the first part thereof; and
(C) mounting said surface mounting device (10) on said printed circuit board (30) with said second surfaces of said first (12) and second (16) lead planes at least partially contacting said first (34) and said second (46) contacts, respectively, and said second surface of the second lead plane (16) at least partially contacting the thermally conductive region (402).

3. The method of claim 2 further characterized by providing a thermally conductive region (402) of a material different than the circuit board (30)

4. A surface mountable (RF) device (10) having low impedance planar contacts, characterized by:
a leadframe (12,14,16) having first (16), second (12) and third (14) spaced-apart portions with gaps therebetween and with coplanar lower surfaces and opposed upper surfaces, wherein the first (16), second (12) and third (14) portions are held in spaced-apart substantially flat relationship by support strips sheared off after encapsulation;
at least one RF transistor die (20) having its lower face bonded tot he upper surface of the first portion (16) and regions on its upper face coupled to the upper surfaces of the second (12) and third (14) portions by electrical connections (26,26′); and
an encapsulation (28) having an upper surface, a lower surface (11) and a side therebetween surrounding the at least one RF transistor die (20) and electrical connections (26,26′), wherein the lower

surface of the encapsulation (11) does not extend beyond the coplanar lower surfaces of the first (16), second (12) and third (14) leadframe portions which are exposed from the lower surface (11) of the encapsulation (28) for providing large area, planar, electrical and thermal contacts to the device (10).

5. The device (10) of claim 4 wherein, after the support strips have been sheared off, the first (16), second (12) and third (14) portions of the leadframe do not protrude substantially beyond the side of the encapsulation (28).

6. A surface mountable RF device (10), characterized by:

a leadframe (12,14,16) of sufficient stiffness to be self supporting and having at least first (16) and second (12) spaced-apart portions with gaps therebetween and with coplanar lower surfaces and opposed upper surfaces, wherein the at least first (16) and second (12) portions are held in spaced-apart relationship by support strips sheared off after encapsulation;

at least one RF semiconductor die (20) having its lower face bonded to the upper surface of the first portion (16) and at least one region on its upper face coupled to the upper surface of the second portion (12) by at least one electrical connection (26); and

an encapsulation (28) having an upper surface, a lower surface (11) and a side therebetween, surrounding the at least one RF semiconductor die (20) and electrical connection (26), wherein the lower surface of the encapsulation (11) does not extend beyond the coplanar lower surfaces of the at least first (16) and second (12) leadframe portions which are exposed on the lower surface of the encapsulation (28).

7. A surface mountable electronic device (10), characterized by:

a metal leadframe (12,14,16) having at least first and second portions with opposed first (16) and second (12) principal surfaces, wherein the second surfaces of the first (16) and second (12) portions are coplanar and exposed;

at least one electronic element (20) having a first face bonded to the first surface of the second portion (12) and another, opposite, face coupled to the first surface of the first portion (16) by electrical connection means; and

molded encapsulation (28) enclosing the electronic element (20) and electrical connection means (26,26′)but not the exposed, coplanar, second surfaces of the first (16) and second (12) portions.

8. The device of claim 7 wherein the leadframe (12,14,16) has a projection measured in the plane of the coplanar second faces, and the encapsulation (28) has a second projection (11) similarly measured, and the first projection does not extend substantially outside the second projection (1

9. An electronic assembly comprising a com tion of a surface mounting electronic device and a circuit board (30) for receiving the de (10) thereon, characterized by:

(A) wherein the surface mounting device (1 comprises, (i) a metal leadframe (12,14,16) ha ing at least first (12) and second (16) portio with opposed first (12) and second surfac wherein the second surfaces of the first (12) a second (16) portions are coplanar, (ii) at le one electronic element (20) having a first fa bonded to the first surface of the second portio (16) and another, opposite, face coupled to the first surface of the first portion (12) by electrical connection means (26), and (iii) a moldec encapsulation (28) enclosing the electronic element (20) and electrical connection means (26) but not the coplanar second surfaces of the first (12) and second (16) portions, wherei the molded encapsulation (28) has a secon surface (11) with the second surfaces of the first (12) and second (16) portions of the leadframe (12,14,16) protruding slightly therefrom;

(B) wherein the circuit board (30) comprises, an electrically insulating substrate (32,33,36) having first (34) and second (46) metal contact regions thereon mating with at least parts of the coplanar second surfaces of the first (12) and second (16) portions of the leadframe (12,14,16), and a highly thermally conductive contact region (40) extending through the electrically insulating substrate so as to mate with another part of the second portion (16) of the leadframe (12,14,16) located immediately beneath the electronic element (20); and

(C) wherein the first (34) and second (46) metal contact regions of the circuit board (30) are bonded to the mating parts of the second surfaces of the first (12) and second (16) portions of the leadframe (12,14,16), and the highly thermally conductive contact region (40) extending through the electrically insulating substrate (32,33,36) is located in intimate thermal contact with the mating another part of the second portion (16) of the leadframe (12,14,16) located immediately beneath the electronic element (20).

10. The assembly of claim 9 wherein the highly thermally conductive contact (40) region is laminated and more thermally conductive than the electrically insulating substrate of the circuit board (30).

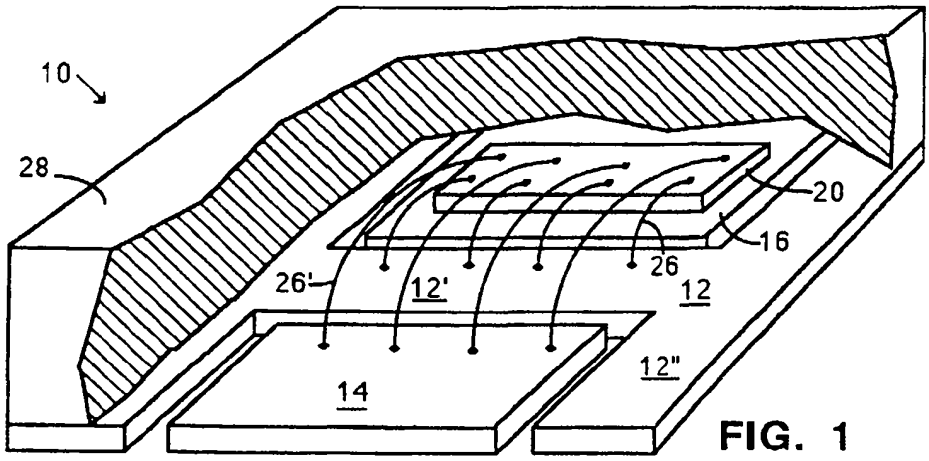

FIG. 1

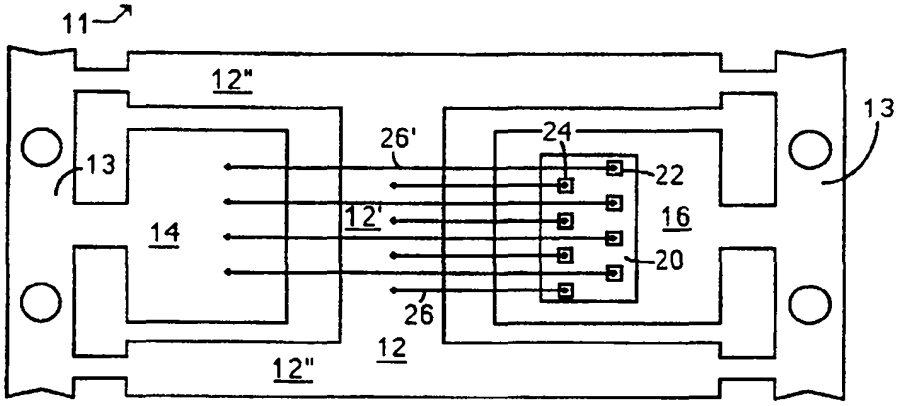

FIG. 2

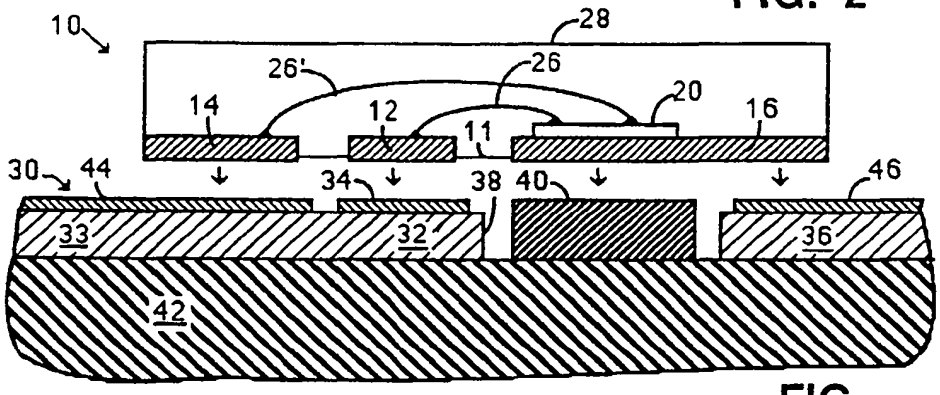

FIG.

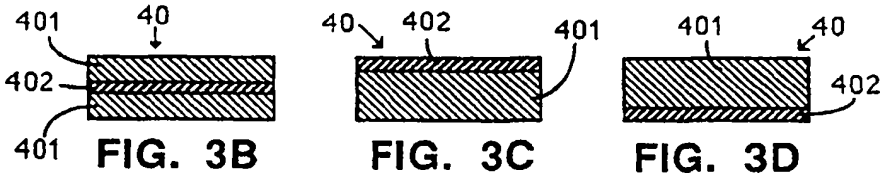

FIG. 3B FIG. 3C FIG. 3D

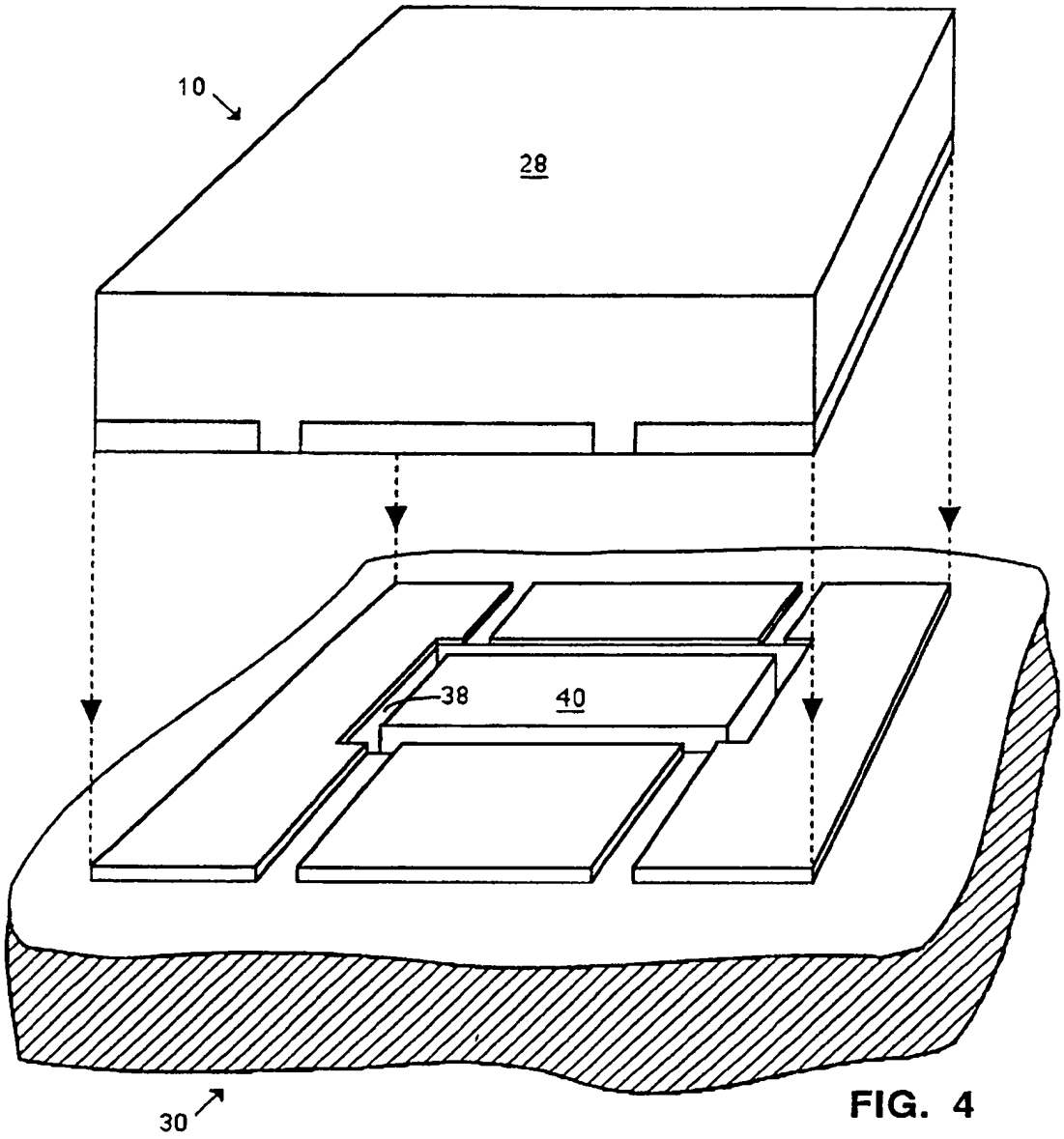

FIG. 4

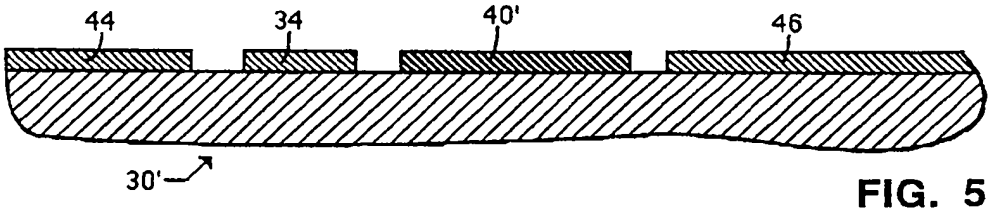

FIG. 5

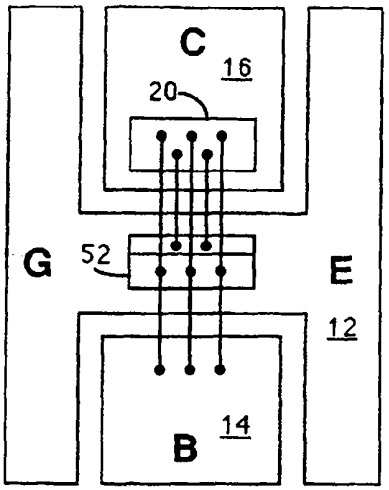

FIG.

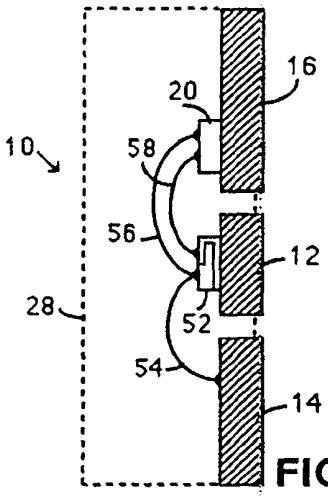

FIG. 6B

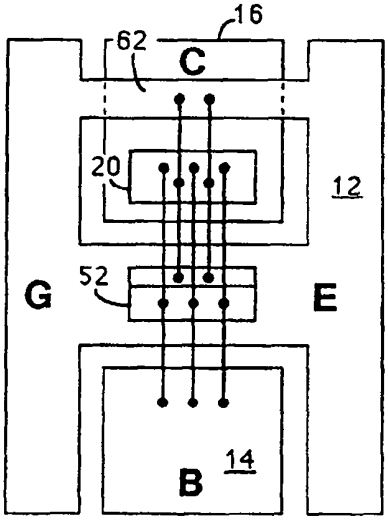

FIG. 7A

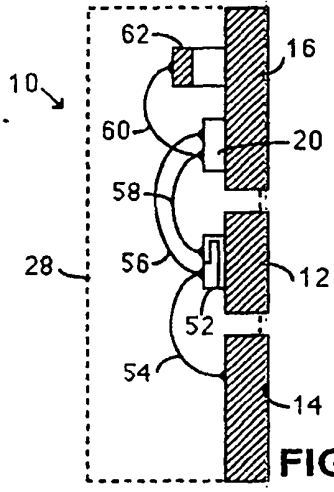

FIG. 7B

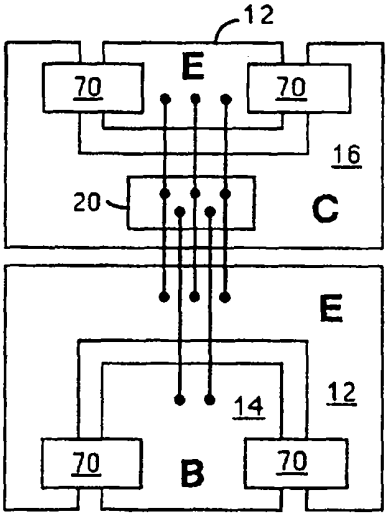

FIG. 8A

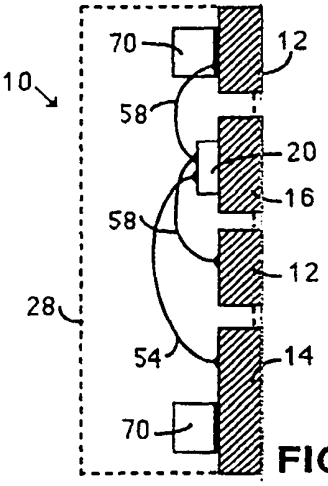

FIG. 8B

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European Patent Office
Office européen des brevets

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(54) **Surface mounting semiconductor device and method.**

(57) A surface mounting device (10) incorporating a high power RF semiconductor transistor comprises a common lead plane (12), an input lead plane (14), a collector lead plane (16), a transistor die (20) electrically and thermally connected to the collector lead plane (16), bonding wires (26,26') for connecting emitters (24) and bases (22) of the transistor (20) to the common (12) and input (14) lead planes respectively, and a molded plastic body member (28) for sealing the device components (70) while leaving the lower coplanar surfaces of the lead planes exposed on the bottom face of the device (11). There are no flying leads.

By eliminating an expensive metallized ceramic insulator from inside the device package (10) and instead providing electrical isolation as a part of an external circuit board (30), the cost for fabricating the device and installing them on the printed circuit board (30) are significantly reduced. The device is particularly rugged and can be easily mounted on the PC board (30) by automated equipment.

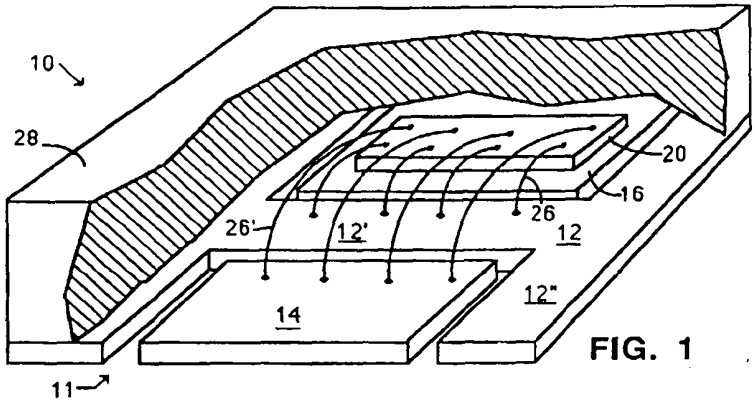

FIG. 1

EP 0 408 904 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 11 1452

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X,Y,A	EP-A-0 211 716 (EUROTECHNIQUE) * column 2, line 43 - column 4, line 44; figures 1, 2 * * ditto * * ditto *	1,7,4-6,8, 2,9	H 01 L 23/66 H 01 L 21/58 H 01 L 25/16
Y	US-A-4 783 697 (BENENATI ROBERT ET AL.) * column 3, line 20 - column 5, line 29; figures 1-4 *	4-6,8	
A	EP-A-0 079 265 (THOMSON-CSF) * page 4, lines 12 - 28; figures 2-4 *	2-4,6,9	
A	EP-A-0 139 431 (LUCAS INDUSTRIES) * page 3, paragraphs 2 - 3; figure 2 *	2,3,9,10	
A	GB-A-2 059 157 (HITACHI) * page 2, lines 10 - 29; figures 3, 12 *	1,4,6,7	
A	FR-A-2 620 275 (THOMSON HYBRIDES ET MICROONDES) * abstract; figures 1, 2 *	1,4,6,7	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 01 L
G 06 K
H 05 K

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
Berlin	24 October 91	LE MINH I

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